IN THE CLAIMS:

1-31. (Canceled)

32. (New) A data writing method used for a semiconductor memory device in which a collective data writing operation is performed using a plurality of memory cell arrays, said data writing method comprising:

latching data at each of a plurality of latch circuits connected to a plurality of bit lines provided on the plurality of memory cell arrays, respectively;

executing a first data writing operation in parallel for the plurality of memory cells connected to each corresponding single word line, for each of the plurality of memory cell arrays with respect to which the collective data writing operation is performed;

verifying the data written in the first data wiring operation, and stopping a data writing operation with respect to a first memory cell array in which writing is completed in all of the memory cells of the plurality of memory cell arrays, at a first time;

executing a second data writing operation for a second memory cell array which is different from the first memory cell array of the plurality of memory cell arrays; and

verifying the data written by the second data writing operation, and stopping the second data writing operation with respect to the second memory cell array in which writing is completed in all of the memory cells of the plurality of memory cell arrays, at a second time later than the first time.

33. (New) The data writing method according to claim 32, wherein said stopping the data writing operations at the first and second time is executed by not applying a write voltage to each corresponding word line.

34. (New) The data writing method according to clam 32, wherein each of the plurality of memory cells includes a non-volatile transistor having a control gate and a floating gate.

35. (New) The data writing method according to claim 32, wherein each of the plurality of memory cell arrays includes a NAND cell in which adjacent memory cells share a common source/drain region.

36. (New) The data writing method according to claim 35, wherein the NAND cell has two ends, each of which has a selective transistor connected.

37. (New) A data writing method used for a semiconductor memory device in which a collective data writing operation is performed using a plurality of memory cell arrays, said data writing method comprising:

latching data at each of a plurality of latch circuits connected to a plurality of bit lines provided on the plurality of memory cells, respectively;

verifying the latched data, and when all of the latched data at corresponding latch circuits connected to a first memory cell array of the plurality of memory cell arrays with respect to which the collective data writing operation is performed are data unnecessary to be written, not executing a writing operation for the first memory cell array;

when the latched data at corresponding latch circuits connected to a memory cell array different from the first memory cell array of the plurality of the memory cell arrays with respect to which the collective data writing operation is performed include data necessary to be written, executing a first data writing operation for the memory cell array different from the first memory cell array.

38. (New) The data writing method according to claim 37, wherein each of the plurality of memory cell arrays includes a NAND cell in which adjacent memory cells share a common source/drain region.

39. (New) The data writing method according to claim 38, wherein the NAND cell has two ends, each of which has a selective transistor connected.

40. (New) The data writing method according to claim 37, further comprising:

verifying data written in the first data writing operation, and stopping writing to a second memory cell array in which writing in all of the memory cell arrays is completed, at a first time,

executing a second data writing operation for a third memory cell array different from the first and second memory cell arrays of the plurality of memory cell arrays; and

verifying data written in the second data writing operation, and stopping writing for the third memory cell array in which writing in all of the memory cell arrays is completed, at a second time later than the first time.

41. (New) The data writing method according to claim 40, wherein said stopping the data writing operations at the first and second time is executed by not applying a write voltage to the word line.